Impact of SFCL on the Four Types of HVDC Circuit Breakers by Simulation

Jong-Geon Lee, Umer Amir Khan, Ho-Yun Lee and Bang-Wook Lee

Abstract— **Recently, studies on HVDC circuit breaker (CB) prototypes have shown successful test results. Nevertheless, effective and reliable solutions regarding massive fault energy during DC fault interruption have not yet been commercialized, and DC current breaking topologies on methods of achieving artificial zero should be somewhat modified. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies. In this work, we studied the application of resistive Superconducting Fault Current Limiters (SFCL) on various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. For the simulation works, four types of DC breaker topologies were modelled including mechanical CB using black-box arc model, passive resonance CB, inverse current injection CB and hybrid HVDC CB. In addition, a resistive SFCL were simulated and added to the DC breakers to verify its interruption characteristic and distributed energy across HVDC CB. From the simulation results, we found that the maximum fault current, interruption time and dissipated energy stress on the HVDC CB could be decreased by applying SFCL. In addition, it was observed that among four types of HVDC CB, passive resonance CB with SFCL exhibited the best observable enhancement.**

Index Terms— **DC Fault Interruption, HVDC Fault, HVDC Circuit Breaker, MTDC, Resistive Superconducting Fault Current Limiter**

I. Introduction

In order to achieve commercial application of future Multi Terminal HVDC (MTDC) networks, typically considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems must be guaranteed [1], [2]. Conventional point-to-point HVDC systems can be sufficiently protected via mechanical circuit breakers located on the AC side [3]; however, a selective coordination protection scheme that isolates faulted lines should be utilized in MTDC to prevent the blackout of the entire grid system [4]. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system [5].

Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption.

To fulfill the zero-crossing condition of DC fault current, a forced current reduction method should be utilized, and various type of HVDC CB are summarized in [6], some of which have revealed prototypes and successful test results. Nevertheless, an effective and reliable solution considering massive fault energy during DC fault interruption is still lacking. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified [7]. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies.

In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers.

Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs.

In order to estimate the performance of combined-application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink. Four types of DC breakers and SFCL were modelled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

II. Modelling of Test-bed, SFCL and HVDC CBs

A. HVDC Test-bed Model

In order to analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed in Matlab /Simulink as illustrated in Fig. 1. The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to concentrate the interruption performance of the

This work was supported by the Human Resources Program in Energy Technology of the Korea Institute of Energy Technology Evaluation and Planning (KETEP), granted financial resource from the Ministry of Trade, Industry & Energy, Republic of Korea. (20154030200730)

This work was also supported by the Power Generation & Electricity Delivery of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) Grant funded by the Korea Government Ministry of Knowledge Economy (No. 2014101050231C).

Jong-Geon. Lee, Umer Amir Khan, Ho-Yun Lee, are with the Division of Electrical System Engineering of Hanyang University, Ansan 426-791, Republic of Korea.

B.W. Lee is with the Division of Electrical Engineering, Hanyang University, Ansan 426-791, Republic of Korea (phone: +82-31-400-5665; e-mail: bangwook@hanyang.ac.kr).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TASC.2016.2542847, IEEE Transactions on Applied Superconductivity

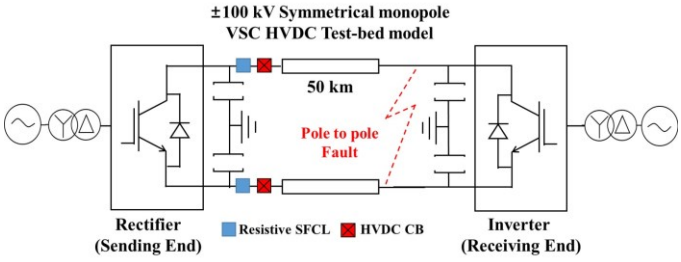

Fig. 1. 2-level point-to-point HVDC test-bed model (V_{ac}: AC voltage, R_{ac}, L_{ac}: system impedance of AC, L_p: Phase reactor)

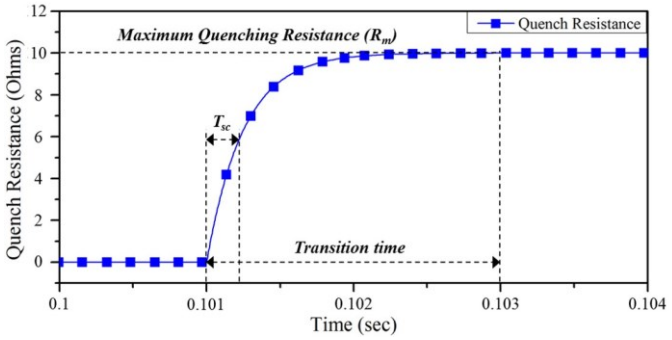

Fig. 2. Quenching characteristics of the designed resistive SFCL with time.

DC fault current in detail. The AC network adjacent to the HVDC link was substituted by an equivalent RL impedance, which enabled the X/R ratio of the power system to be determined. The converter transformer was a wye-delta connection. A phase reactor, L_p, was added between the converter and transformer to filter the harmonics during conversion. Each type of HVDC CB and SFCL was located at the output of the rectifier. Detailed specifications of the HVDC link are as follows: the rated voltage = ±100 kV, nominal current = 1 kA, nominal power flow = 100 MW, and the transmission line length = 50 km.

B. Resistive Superconducting Fault Current Limiter

The resistive SFCL, which is based on the quenching phenomena of superconductors, has been an area of great interest for researchers in the last decade [9], and several prototypes have been developed and installed in medium- and high-voltage systems [10]. Focusing on the theoretical approaches for a resistive SFCL [11], the quenching phenomena of SFCL can be expressed as:

$$R_{SFCL}(t)=\begin{cases}0 & (t<t_{quenching})\\ R_m(1-\exp(-t/T_{sc})) & (t_{quenching}<t)\end{cases} \quad (1)$$

where R_m is the maximum quenching resistance, and T_{SC} is the time constant for the transition to the quenching state. In this work, the SFCL rating was 100 kV DC with a 2 kA of critical current. The maximum quenching resistance, R_m, is 10 Ω.

Until now, there is no practical applications of DC SFCL. Therefore, in order to determine the transition time, which refers to the elapsed time from zero resistance to maximum quench resistance of resistive SFCL, the transition time of AC SFCL was referred. It should be determined within 1/2 cycle, and therefore the transition time of designed SFCL was assumed to 2 ms [12]-[14]. In addition, in order to acquire nearly 10 ohms of R_q within 2 ms, the value of T_{sc} was determined to 0.25 ms. The quenching characteristics of the designed SFCL based on (1) are shown in Fig. 2.

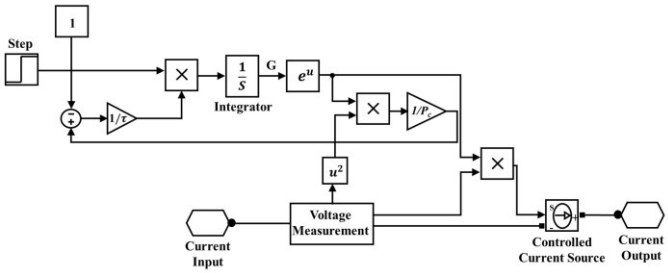

Fig. 3. The modified Mayr black-box arc model designed using Matlab/ Simulink for discrete simulation environment.

C. Arc Modeling

The representative HVDC CB topologies are categorized as follows: mechanical CB (MCB), passive resonance CB (PRCB), inverse current injection CB (I-CB) and Hybrid DC CB (HDCCB) [15]. Except for the non-arc type such as inverse current injection and Hybrid DC CB, the implementation of arc dynamics is a major concern in the design for an accurate simulation model. The black-box arc model, which represents the arc dynamics by calculating the differential equation of the arc conductance, was designed.

We considered the Mayr and Cassie models as black-box arc models; models are based on the energy balance equation, which describes the change in the arc column's energy content resulting from the imbalance between ohmic heating and forced cooling [16]. In our simulation model, the modified Mayr black-box arc model was used for MCB, which assumes arc conductance, g, arc cooling power, $P_c(g)$, and arc time constant, τ, as shown in (2), [17]:

$$\frac{1}{g}\frac{dg}{dt}=\frac{d\ln g}{dt}=\frac{1}{\tau(g)}\left(\frac{ui}{P_c(g)}-1\right) \quad (2)$$

The advantage of the modified Mayr arc model is that it is able to determine the breaking capability of MCB by controlling $P_c(g)$. To determine the $P_c(g)$ and τ, following equations and parameters in Table I were used [18], [19]:

$$P_c(g)=p\cdot P_0\cdot g^a, \quad (3)$$

$$\tau(g)=\tau_0\cdot g^b. \quad (4)$$

where P_0 is the constant cooling power factor which depends linearly on the blow pressure p.

While various black-box arc models already exist in Matlab/Simulink, they only consider the continuous model environment [20]. Due to the complicated nature of the system, a discrete model is required to accomplish an efficient simulation. To implement the continuous black-box arc model into Matlab/Simulink in discrete model, (2) was transformed into integral form as (5) and the simulation model was designed as shown in Fig. 3.

$$g=\int_0^t\frac{1}{\tau}\left(\frac{i^2}{P_c(g)}-g\right)dt. \quad (5)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TASC.2016.2542847, IEEE Transactions on Applied Superconductivity

TABLE I
PARAMETERS OF DESIGNED BLACK-BOX ARC MODEL

Parameter	Value
P_0	0.393 MW
p	70 bar
a	0.25
τ_0	15 μsec
b	0.5

D. Modelling of HVDC CBs

The concepts of HVDC CB are classified in CIGRE WG. B4.52 according to the method to achieve artificial current zero to interrupt fault current [15]. The simulation models of HVDC CBs in our simulation were designed as follows;

Mechanical CB (MCB): This concept has been used for low-voltage DC breakers of few kilovolts only, which is usually in air-blast CB or SF6 CB [18]. In case of MCB, a DC current is reduced by increasing the arc voltage to higher value than that of the system voltage. By utilizing the designed black-box arc model, the simulation model of MCB was designed as shown in Fig. 4(a). In order to achieve the practical approach of simulation results, the delay time was assumed as 10 ms.

Passive resonance CB (PRCB): To dissipate the energy stress on the MCB, the secondary path with a series L-C circuit is added as shown in Fig. 4(b). When the fault occurred at 0.1 sec, MCB opens with 10 ms of delay considering opening delay, and then an arc forms across the contacts with increasing arc impedance. The DC current begins to commutate and resonate in the secondary path after the arc impedance exceeds the L-C impedance. When a DC current of the primary path meets zero crossing, a current through the MCB can be interrupted by the extinction of the arc. An additional parallel surge arrester (SA) circuit is supplemented to prevent voltage stress across the PRCB during arc extinction.

Inverse current injection CB (I-CB): This scheme is similar to PRCB. However, the pre-charged capacitor via an additional DC power source injects an inverse current into the primary path after the current commutates to secondary path as shown in Fig. 4(c). This can reduce the interruption and oscillation time when compared to that of PRCB.

Before a fault, a charging switch (ACB1) and an auxiliary switch (ACB2) maintains closed state. Thereby capacitor can be charged by DC source. When a fault occurs, after an 10 ms delay, MCB and ACB1 contacts open simultaneously. Then the high discharging inverse current from capacitor is supplied to main path. The fault current is rapidly decreased and transient recovery voltage appears between the terminals of I-CB. When the voltage exceeds to the knee voltage of SA, it is triggered to restrain the voltage rise, and it absorbs the fault energy. After 3 ms from the time when MCB and ACB1 were opened, ACB2 is triggered and it isolates the secondary path. This opening of ACB2 will prevent the current to flow through the secondary path which could make additional LC resonance current. Therefore, remaining fault energy is exclusively absorbed by SA. If the current reaches to zero, a residual circuit breaker (RCB) opens and the current interruption is complete.

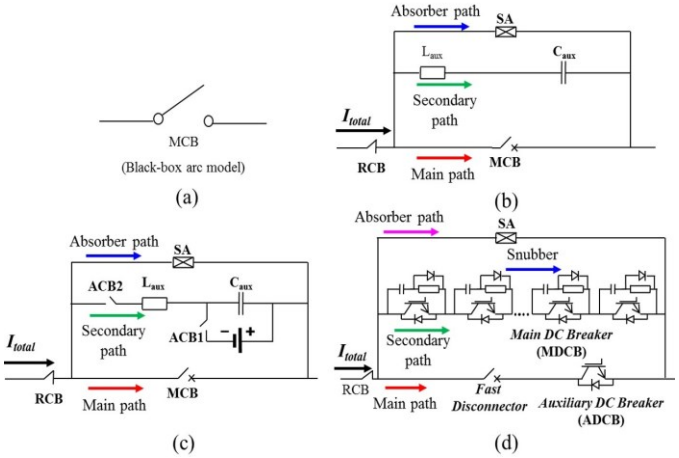

Fig. 4. HVDC CB models: the (a) Mechanical CB (MCB), (b) Passive resonance CB (PRCB), (c) Inverse current injection CB (I-CB), and (d) Hybrid DC CB (HDCCB).

Hybrid DC CB (HDCCB): This scheme is widely considered as the optimal concept for interrupting DC fault current, was designed as illustrated in Fig. 4(d) [21]. The delay times of IGBT was assumed as Δt_{IGBT} = 6 μs in simulation.

When a DC fault occurs, the auxiliary DC breakers (ADCB) and fast disconnector are opened sequentially, then the current starts to commutate from the main path to secondary path. After commutation, main DC circuit breakers (MDCB) in secondary path are opened, and total current is reduced because the current flows to the snubber circuit of MDCB until the parallel-connected SA trips. When the voltage across the HDCCB terminals exceed to knee voltage, the SA ignites and forces the DC fault current to zero by absorbing remaining fault energy. Finally, a RCB opens and isolates the DC fault.

III. SIMULATION ANALYSIS AND DISCUSSION

Transient fault simulations were conducted to analyze the effects of SFCL on various HVDC CB types. Each type of HVDC CB, both with and without SFCLs, was applied at the sending end of the test-bed.

A pole-to-pole fault, which considered a severe fault in HVDC systems, was generated on the receiving end at 0.1 sec. The prospective maximum fault current without any protection devices was 14.7 kA in the designed test-bed. The rising rate of the fault current di/dt during early 10 ms was measured as 589 A/ms. Therefore, considering high rising rate of the fault current, fast interruption should be achieved.

A. Case 1: Mechanical CB (MCB)

Fig. 5 shows the DC fault interruption performance of the MCB. A maximum prospective fault current was measured as 14.7 kA. Without SFCL, fault current was reduced from 14.7 kA to 13.8 kA. Arc extinction could not be achieved due to low cooling power, $P_c(g)$, and a slight current reduction was measured due to the generation of arc resistance.

In the case of 'with SFCL', a 67.3 % current reduction from 14.7 kA to 4.8 kA was observed, but fault interruption was still not achieved. To interrupt the DC fault current utilizing the MCB only, the arc cooling power, $P_c(g)$, should be increased; however, it is difficult to fulfill the insulation

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TASC.2016.2542847, IEEE Transactions on Applied Superconductivity

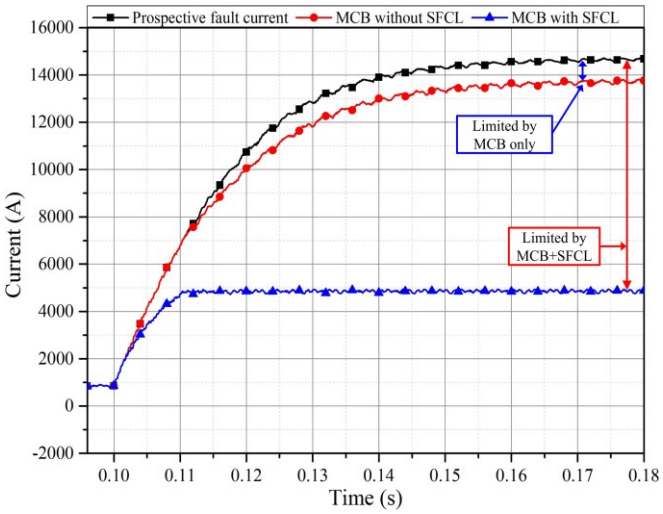

Fig. 5. Interruption characteristics of MCB when SFCL was applied.

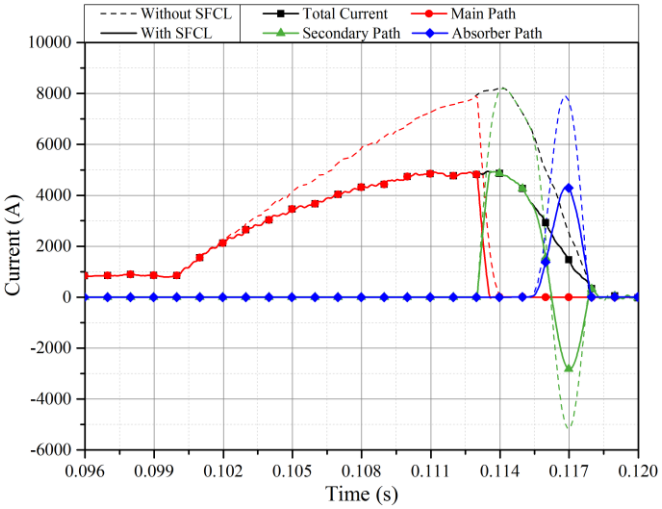

Fig. 7. Interruption characteristics of the I-CB when SFCL was applied.

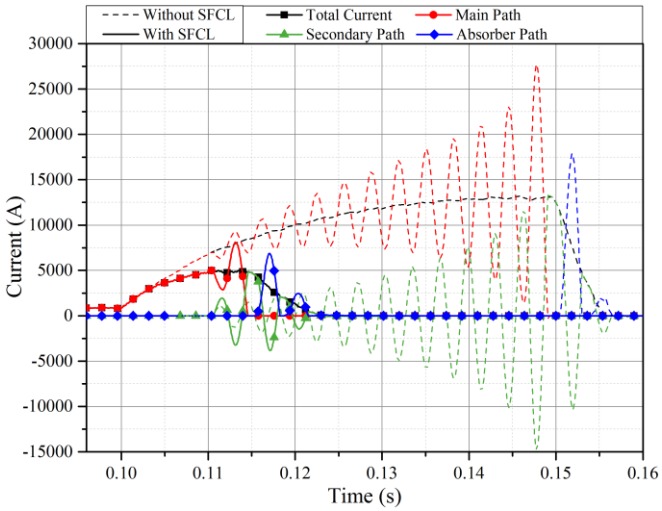

Fig. 6. Interruption characteristics of PRCB when SFCL was applied.

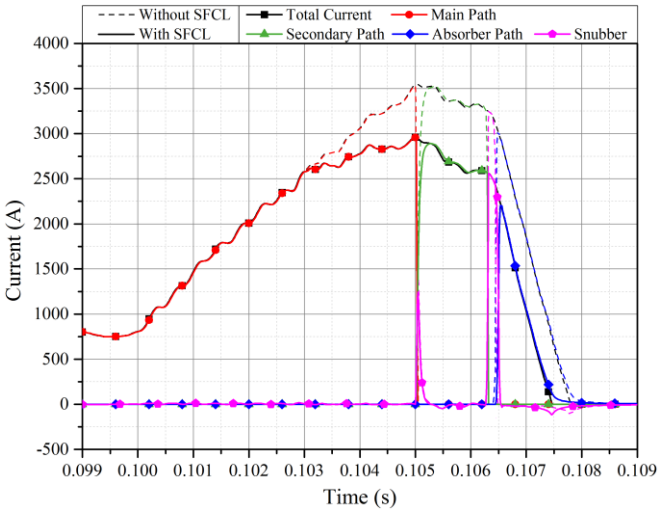

Fig. 8. Interruption characteristics of the HDCCB when SFCL was applied.

requirement, particularly in high-voltage application. In addition, DC fault interruption was not achieved in spite of the application of SFCL. Therefore, it was deduced that DC fault interruption via the MCB was not an appropriate solution to clear DC fault.

B. Case 2: Passive Resonance CB (PRCB)

Fig. 6 shows the DC fault interruption performance of the PRCB. Without SFCL, the maximum fault current intensity (I_{total}) was measured at 13.2 kA, and the maximum current in the main path reached 27.5 kA owing to resonant oscillation. The total interruption time was 55 ms. In this regard, considering the fast *di/dt* of the DC fault current, using PRCB alone was not an appropriate solution to clear fault within a short time span.

After applying SFCL, the maximum I_{total} was 5 kA; 62.1 % of the fault current was decreased. As the impedance of the main path increased via SFCL quenching, the time constant L/R of the test-bed declined, enabling the reduction of total oscillation time. Thus, fast interruption was achieved within 25 ms with less oscillation, and if faster interruption time is required, increasing the quench resistance could be a solution by reducing the time constant of the secondary path.

C. Case 3: Inverse current injection CB (I-CB)

Fig. 7 presents the interruption characteristics of the inverse current injection CB (I-CB). Without SFCL, the maximum I_{total} was 8.2 kA, which is lower than that of the PRCB. Unlike the interruption characteristics of the PRCB, no oscillation was observed in the I-CB, because discharge of the pre-charged capacitor supplies large inverse current over a short duration. Therefore, a fast I-CB interruption time, measured at 18 ms, was achieved as compared to that of PRCB.

In the case of 'with SFCL', the maximum I_{total} was 4.9 kA. Interruption time was equal to the case without SFCL. There was no passive oscillation with the inverse current injection over a short duration; therefore, unlike PRCB, the L/R time constant on the secondary path did not influence on the interruption characteristics of the I-CB.

D. Case 4: Hybrid DC CB (HDCCB)

The primary characteristic of the HDCCB is that it achieves fast interruption due to the response time of a semi-conductor. The maximum I_{total} found was 3.5 kA, and the interruption time was 7.8 ms, which is the lowest value depicted in Fig. 8. By applying SFCL, the maximum I_{total} = 2.9 kA, which is the lowest value with a 17.1 % reduction ratio and estimated

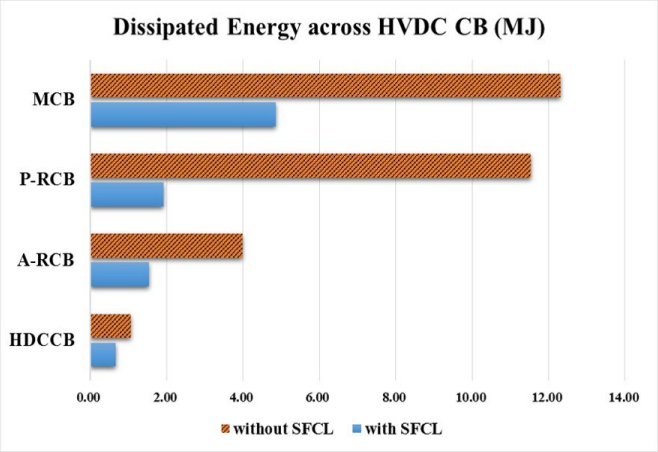

Fig. 9. Comparison of dissipated energy across the HVDC CB during a fault.

TABLE II
IMPACT OF RESISTIVE SFCL ON FOUR TYPES OF HVDC CB

	MCB	PRCB	I-CB	HDCCB
Reduced I_{total} (%)	67.3	62.1	40	17.1
Reduced Δt_{int} (ms)	No Interruption	30	0	0.2
Reduced E_{fault} (%)	60.5	83.4	61.2	37.4
Required components	MCB (+SFCL)	MCB, LC, SA (+SFCL)	MCB, ACB,LC, SA, S_{DC} (+SFCL)	IGBTs, MCB, ACB,SA (+SFCL)
Cost	*	**	***	****

I_{total}: total current, Δt_{int}: interruption time, E_{fault}: dissipated energy during a fault, *SA*: Surge Arrestor, *LC*: LC Impedance, ACB: Auxiliary CB, S_{DC}: DC source, *: the cost, which is referenced on the development cost of MCB

interruption time of 7.6 ms. Regarding the fast response of HDCCB, the circuit interruption has been progressed within the transition time of SFCL. Therefore, we determined that the effect of SFCL on a HDCCB exhibits insufficient performance as compared to other concepts.

E. Analysis of energy dissipation

Energy dissipation is the primary design parameter used to determine the breaking capability of CB. In this study, dissipated energies on SFCL and HVDC CBs were calculated. From (6), the measured current, voltage and total interruption time determine the dissipated energy across the HVDC CB:

$$E_{dissipated} = \int_{t\_fault}^{t.interruption} Pdt = \int_{t\_fault}^{t.interruption} V_{cb} Idt \,. \qquad (6)$$

where the V_{cb} is the voltage across HVDC CB during a fault interruption.

Fig. 9 shows the dissipated energy across the CB both with and without application of the SFCL. Without the SFCL, the highest energy dissipation was observed in the MCB due to interruption failure, and the lowest energy dissipation was observed in the HDCCB. By applying the SFCL, energy reduction was observed from all types of HVDC CB. Among these, PRCB with SFCL showed the best performance with an 83.4 % energy reduction; however, the SFCL shows less effect on the HDCCB, which is considered the best concept among the HVDC CBs.

To determine the optimum topology for HVDC CBs with SFCL, comparative analyses were conducted considering the interruption performance and cost, as shown in Table II. The best performance improvement was achieved via the PRCB. I-CB also resulted in improvement, though still less than that of the PRCB.

Maintenance of the I-CB is complicated due to the external power source needed to charge the auxiliary capacitor. The HDCCB, which showed the highest performance of all, has a disadvantage in its high development cost. In addition, a few HDCCB performance improvements were observed if the SFCL was applied. Exclusive use of the HDCCB was the optimum solution to achieve DC current interruption through the HDCCB, considering cost effectiveness. PRCB, which is considered the least efficient HVDC CB concept, has shown the noticeable enhancement by applying SFCL considering the fault interruption capability and development cost.

IV. CONCLUSION

This paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC test-bed were designed using Matlab/Simulink. A severe DC pole-to-pole fault was imposed to analyze the interruption performance.

From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and highest maximum fault current without SFCL. When the SFCL was applied, the L/R time constant of the secondary path was decreased, and therefore fast interruption with less oscillation was observed. Consequently, SFCL installation with PRCB could be a viable, reliable, and cost-effective option to enhance DC fault current interruption capability.

REFERENCES

[1] Yidong Hong and Tao Yu, "Reliability improvement strategies for HVDC transmission system," *Energy and Power Engineering*, vol. 5, no. 3B, pp. 52-56, May 2013.

[2] J. Yang, J. Fletcher, and J. O'Reilly, "Multi-terminal DC wind farm collection grid internal fault analysis and protection design," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2308-2318, Oct. 2010.

[3] L. Tang, *et al.,* "Protection of VSC multi-terminal HVDC against DC faults," in *Proc. 33rd Annual IEEE Power Electronics Specialist Conference*, vol.2, pp.719-724, Jun. 2002.

[4] J. Rafferty, L. Xu and D. J. Morrow, "DC fault analysis of VSC based multi-terminal HVDC systems," in *Proc. AC and DC Power Transmission(ACDC 2012), 10th IET International Conference on*, pp.1-6, Dec. 2012

[5] C. M. Franck, "HVDC circuit breakers: a review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998-1007, Apr. 2011.

[6] K. Tahata, *et al.,* "HVDC circuit breakers for HVDC grid applications", in *Proc. CIGRE AORC Tech. Meeting*, Tokyo, Japan, May 2014.

[7] R. Zeng, *et al.,* "Precharging and DC fault ride-through of hybrid MMC-based HVDC system," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1298-1306, Jun. 2014.

[8] Steven M. Blair *et al.,* "Analysis of energy dissipation in resistive superconducting fault current limiters for optimal power system performance," *IEEE Trans. Appl. Supercond.*, vol. 21, no 4, pp. 3452-3457, Aug. 2011.

[9] Umer Amir Khan, *et al.,* "A novel model of HVDC hybrid-type superconducting circuit breaker and its performance analysis for limiting and breaking DC fault current," *IEEE Trans. Appl. Supercond*., vol. 25, no. 6, Dec. 2015, Art. ID. 5603009.

[10] H. Kim *et al.,* "Development and grid operation of superconducting fault current limiters in KEPCO," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 5, Oct. 2014, Art. ID. 5602504.

[11] H. J. Lee *et al.,* "Effect of a SFCL on commutation failure in a HVDC system," *IEEE Trans. Appl. Supercond.*, vol. 23, no 3, Jun. 2013, Art. ID. 5600104.

[12] M. Noe and M. Steurer, "High-temperature superconductor fault current limiters: Concepts, applications, and development status," *Supercond. Sci. Technol.*, vol. 20, no. 3, pp. R15-R29, Jan. 2007.

[13] Y. Shirai *et al.*, "Simulation study on operating characteristics of superconducting fault current limiter in one-machine infinite bus power system," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 1822–1827, Jun. 2003.

[14] Umer Amir Khan *et al.,* "Feasibility analysis of the application and positioning of DC HTS FCL in a DC microgrid through modeling and simulation using Simulink and Simpowersystem," *Phys. C, Supercond.*, vol. 471, no. 21-22, pp. 1322–1326, Nov. 2011.

[15] CIGRE Working Group B4.52 "HVDC grid feasibility study: appendix H", *International Council for Large Electric Systems (CIGRE), Technical Brochure 533*, Apr. 2013.

[16] O. Mayr, "Beiträge zur theorie des statischen und des dynamischen lichtbogens," *Arch. Elektrotech.*, vol. 37, no. 12, pp. 588–608, Dec. 1943.

[17] Pieter H. Schavemaker, Lou van der Sluis, "An improved Mayr-type arc model based on current-zero measurements", *IEEE Trans. Power Del.*, Vol. 15, no. 2, pp. 580-584, Apr. 2000.

[18] M. Bucher, C. M. Frank, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 87-95, Feb. 2015.

[19] M. M. Walter, "Switching arcs in passive resonance HVDC circuit breakers," Ph.D. dissertation, ETH, Zurich, 2013. [Online]. Available: DOI: 10.3929/ethz-a-010112102.

[20] P. H. Shavemaker, *et al.,* "The arc model blockset", in *proc. The second IASTED international conference power and energy system (EuroPES)*, Crete, Jun. 2002.

[21] M. Callavik *et al.,* "The Hybrid HVDC breaker," *ABB Grid Systems, Technical paper*, Nov. 2012.